Back-Illuminated SPAD With Jitter Optimization

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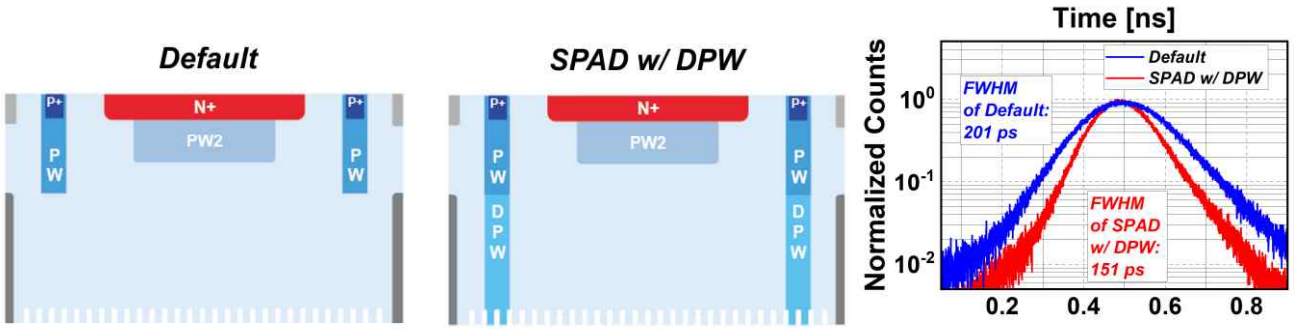

(a) (b) (c)

Fig. 1. (a) Default SPAD, (b) SPAD with DPW, and (c) measured timing-jitter results of the SPADs.

We demonstrate timing-jitter optimization in non-isolated single-photon avalanche diodes (SPADs) fabricated in a backside-illumination (BSI) 90 nm CMOS image sensor (CIS) foundry technology by engineering the anode-side electrostatic potential using a deep p-well (DPW). The proposed engineering enhances the electric field in the drift region, improving carrier transport toward the avalanche initiation area and thereby enabling faster and more consistent avalanche triggering.

As shown in Fig. 1, both SPADs are based on an N+/p-well (PW) junction, and partial DTI combined with STI is placed on both sides of the SPADs. Moreover, backside patterning is incorporated to increase the optical path length, thereby enhancing charge-collection efficiency at near-infrared (NIR) wavelengths. The baseline device, referred to as the Default SPAD (Fig. 1(a)), employs only a PW implant at the anode. In contrast, the proposed device, denoted as the SPAD w/ DPW (Fig. 1(b)), introduces an additional DPW underneath the anode PW. The DPW modifies the potential distribution such that the effective bias influence extends deeper and toward the backside surface. Consequently, the drift-assisted transport region is enlarged, and the carrier drift components toward the high-field multiplication region are increased. This bias extension reduces the transit-time spread of photo-generated carriers, mitigates timing variations associated with carriers generated at remote locations, and improves the uniformity of carrier collection across the active volume. In addition, the DPW structure enhances the anode-side current path and charge supply during avalanche buildup, resulting in an avalanche current increase and thereby producing a steeper rising edge of the output pulse. In the threshold-based timing readout, timing uncertainty induced by frontend noise is reduced when the output signal rises more rapidly, because a steeper edge decreases the event-to-event variation of the threshold-crossing instant.

Fig. 1(c) compares normalized timing histograms (counts versus time) for the two structures measured at room temperature under the excess bias of 5 V. The SPAD w/ DPW clearly exhibits a narrower distribution than the Default SPAD. Quantitatively, the full width at half maximum (FWHM) improves from 201 ps for the Default SPAD to 151 ps for the SPAD w/ DPW, corresponding to an approximately 25% reduction in timing jitter.

The results confirm that DPW-assisted anode potential engineering is an effective and process-compatible technique for improving temporal resolution in backside-illuminated Non-isolated type SPADs, and is particularly attractive for short-to-mid-range light detection and ranging (LiDAR) systems requiring low jitter, such as mobile, VR/AR, and AI robots.

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